ABSTRACT OF THE DISCLOSURE

A technique for testability of a semiconductor integrated circuit is disclosed. In a first step, a fault simulation is conducted based on a predetermined test pattern to discriminate detectable faults and undetectable faults from each other. In a second step, undetected faults are listed. In a third step, the test conditions for the undetected faults are determined. In a fourth step, a test pattern most likely to meet the test conditions is selected from among a plurality of test patterns. In a fifth step, the registers associated with the undetected faults are replaced with scan registers, while at the same time connecting the scan registers in a scan chain to thereby make up a modified circuit. In a sixth step, a fault simulation is conducted by switching to the test condition at the timing corresponding to the undetected faults using the test pattern for the modified circuit.